

FIG.1A

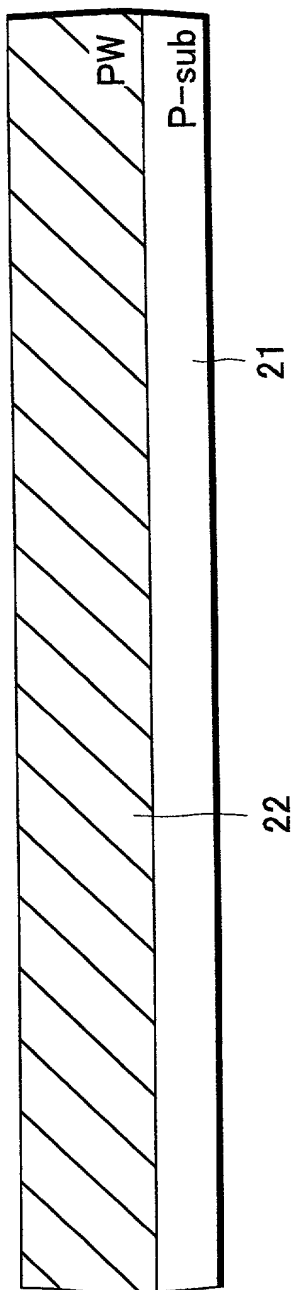


FIG.1B

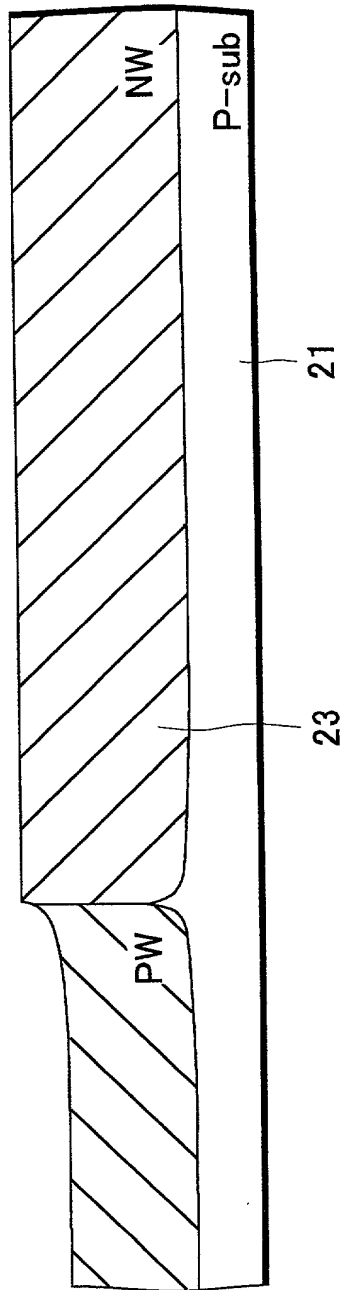


FIG.2A

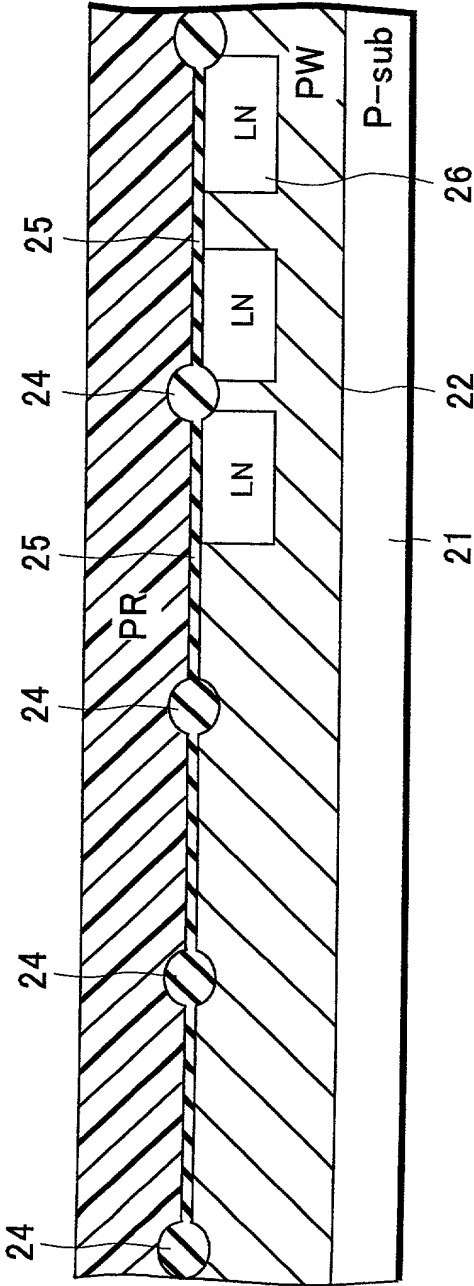


FIG.2B

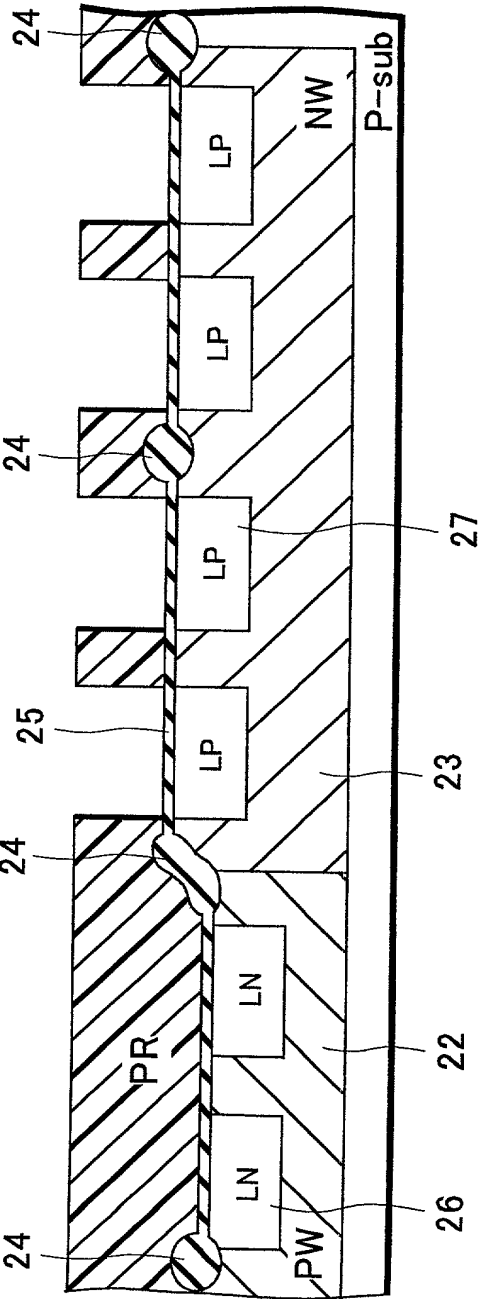


FIG.4A

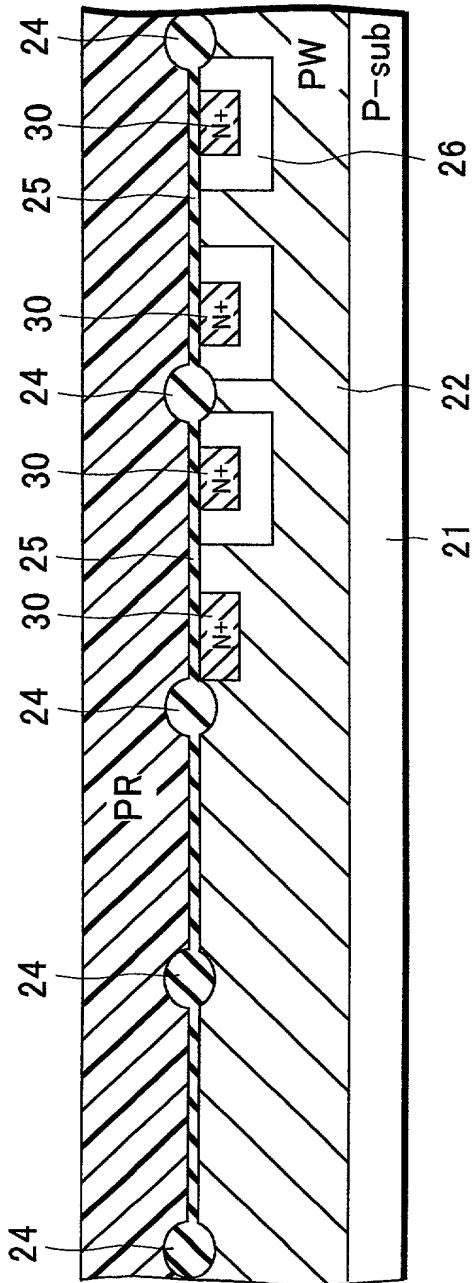


FIG.4B

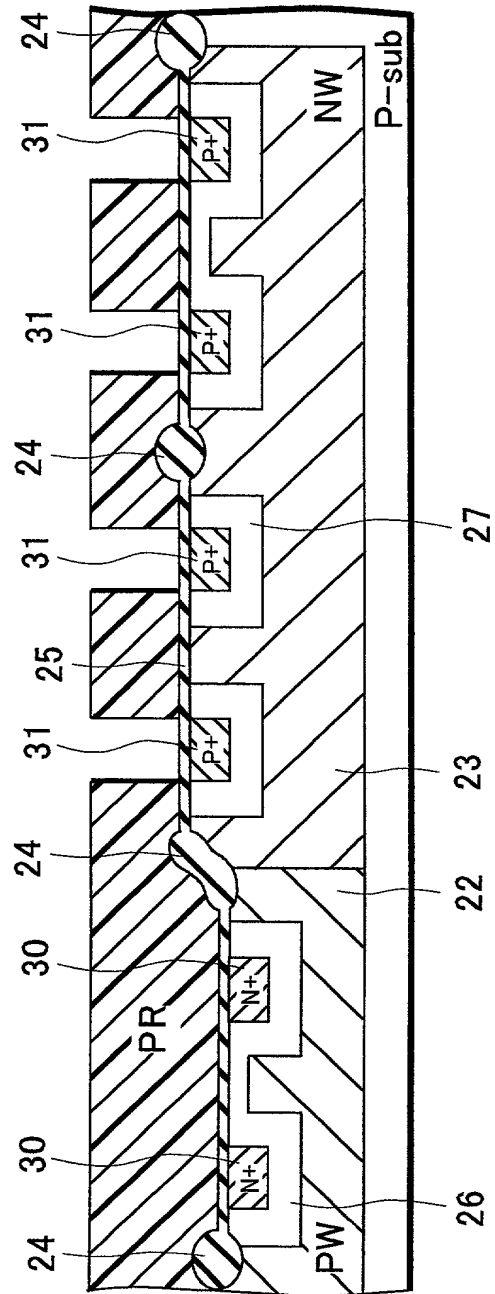


FIG.5A

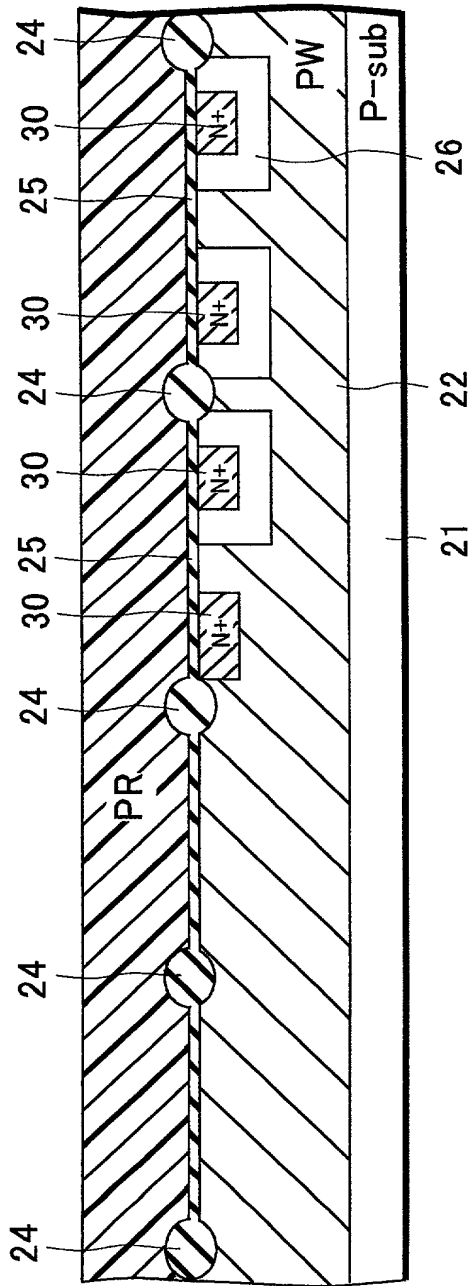


FIG.5B

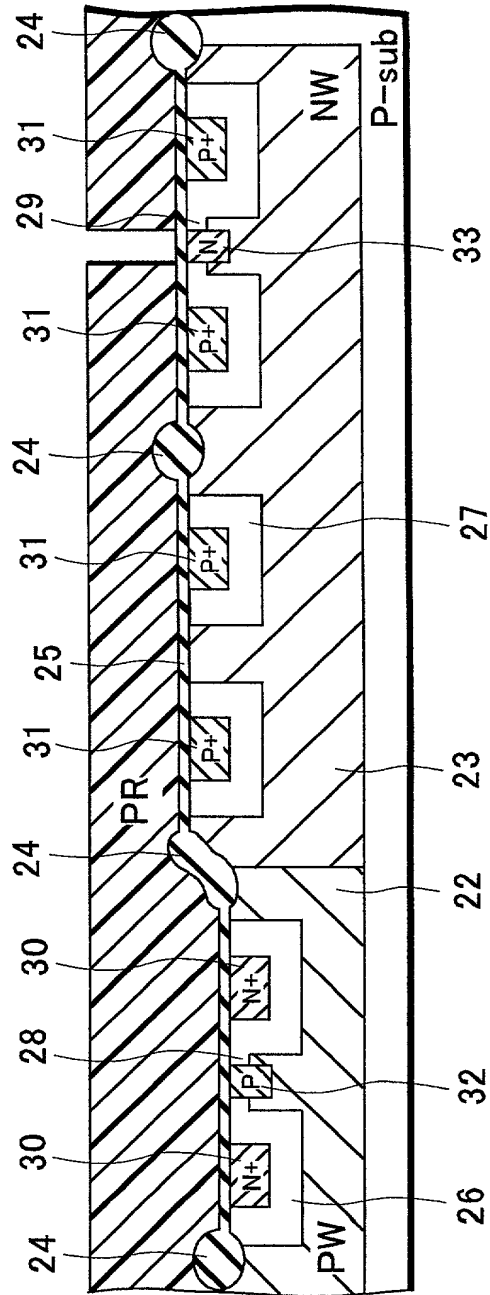


FIG.6A

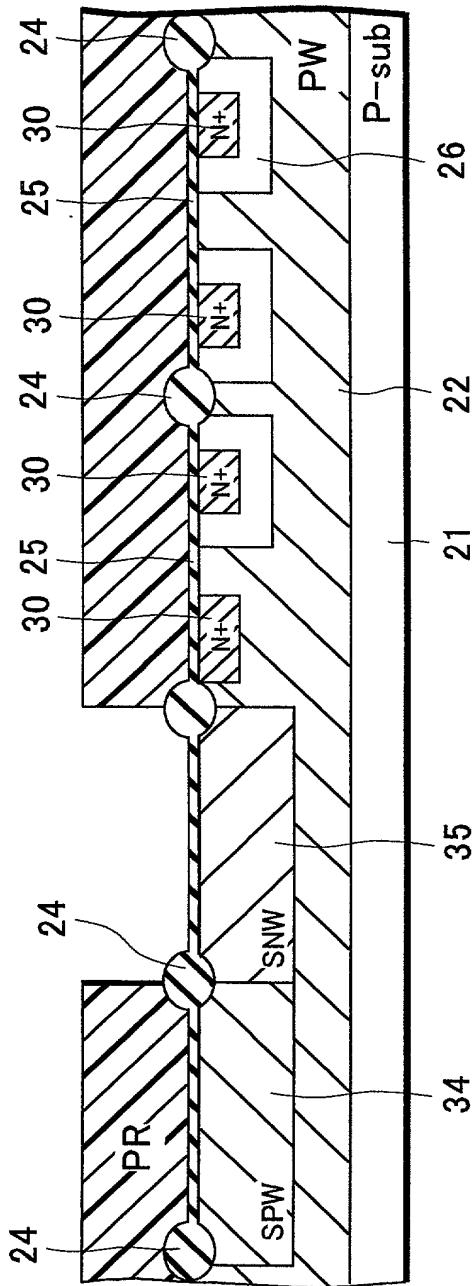


FIG.6B

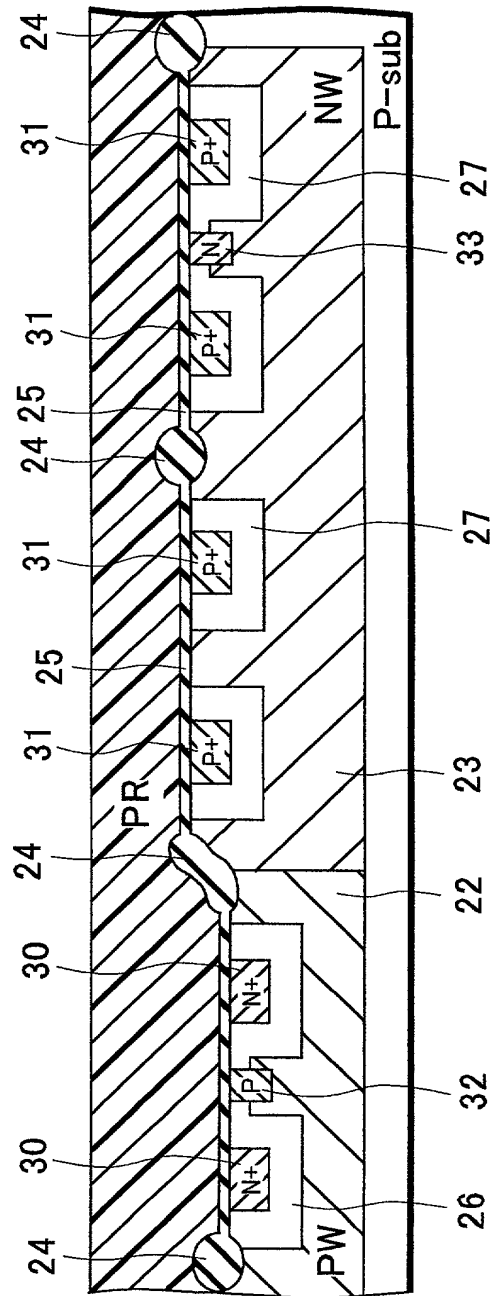


FIG. 7A

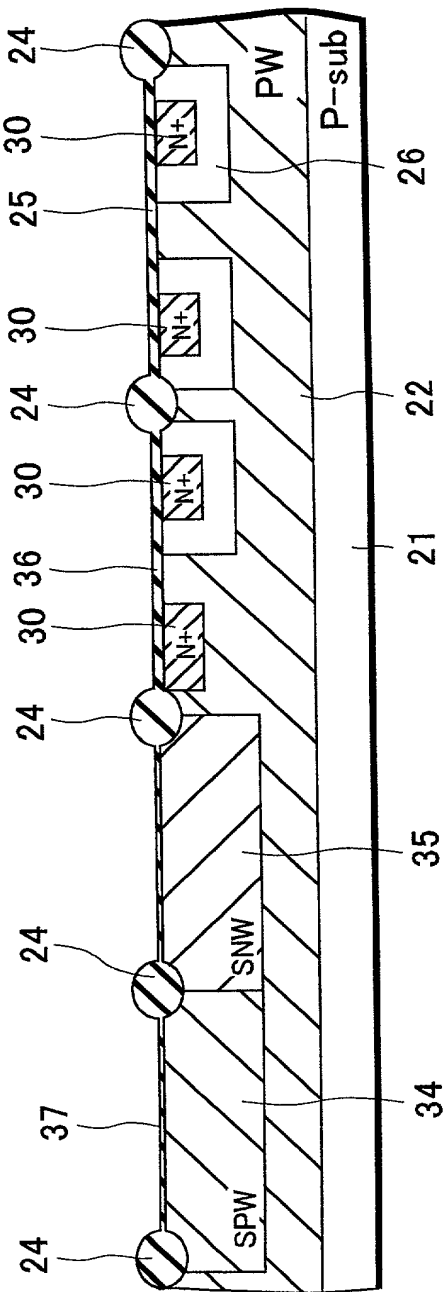


FIG. 7B

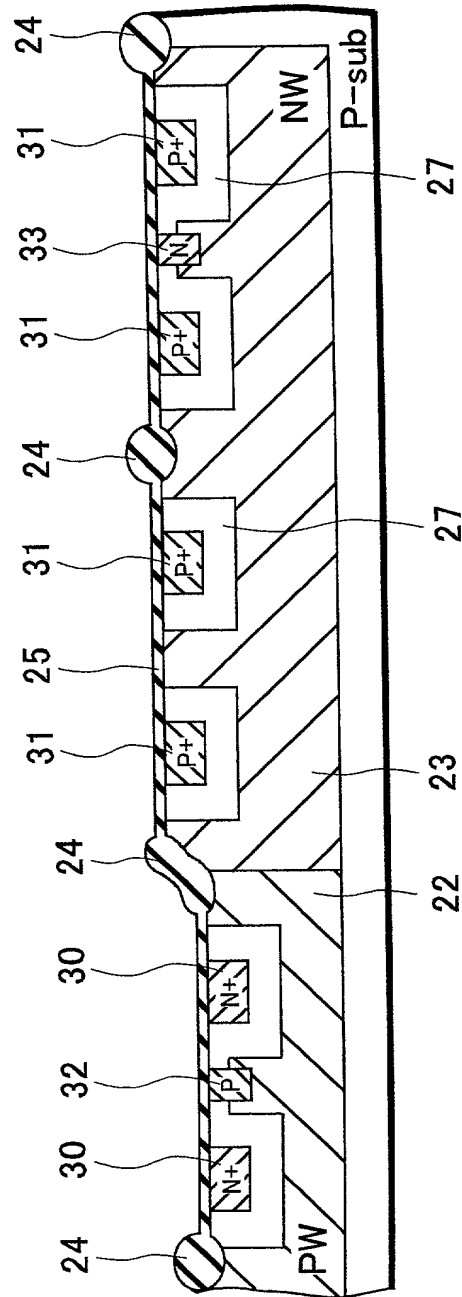


FIG.8A

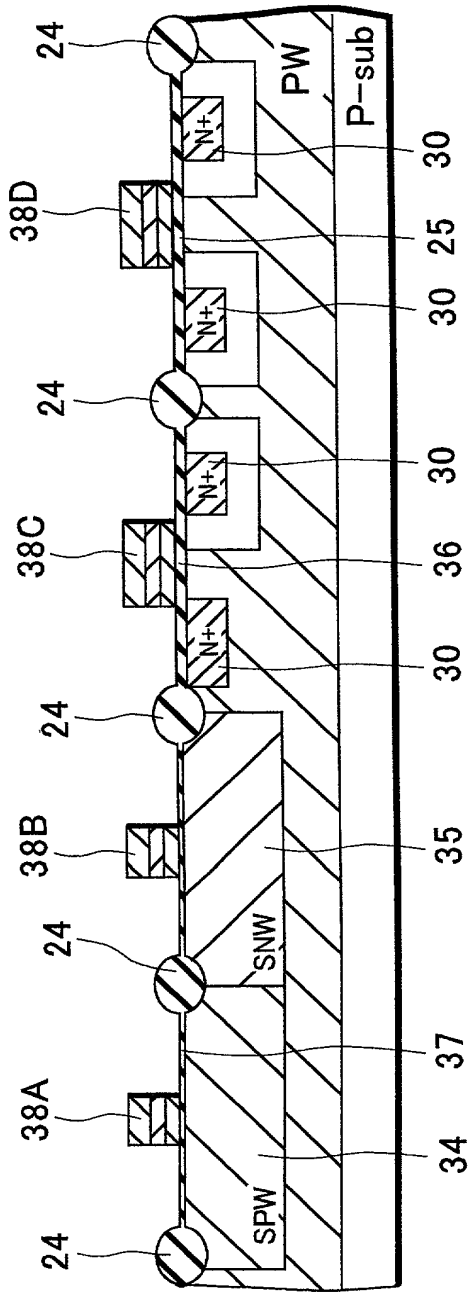


FIG.8B

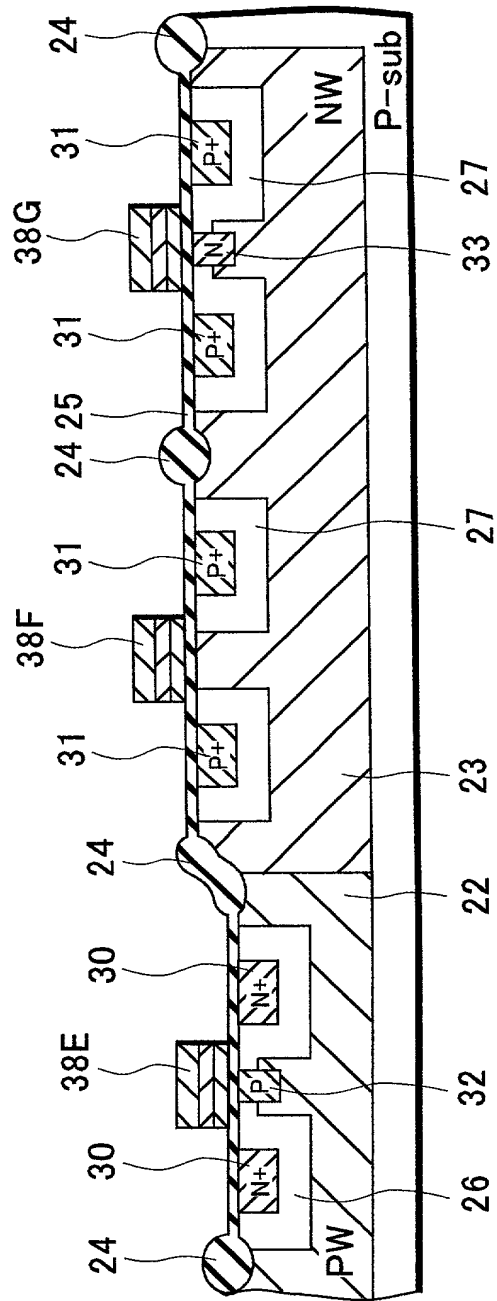


FIG.9A

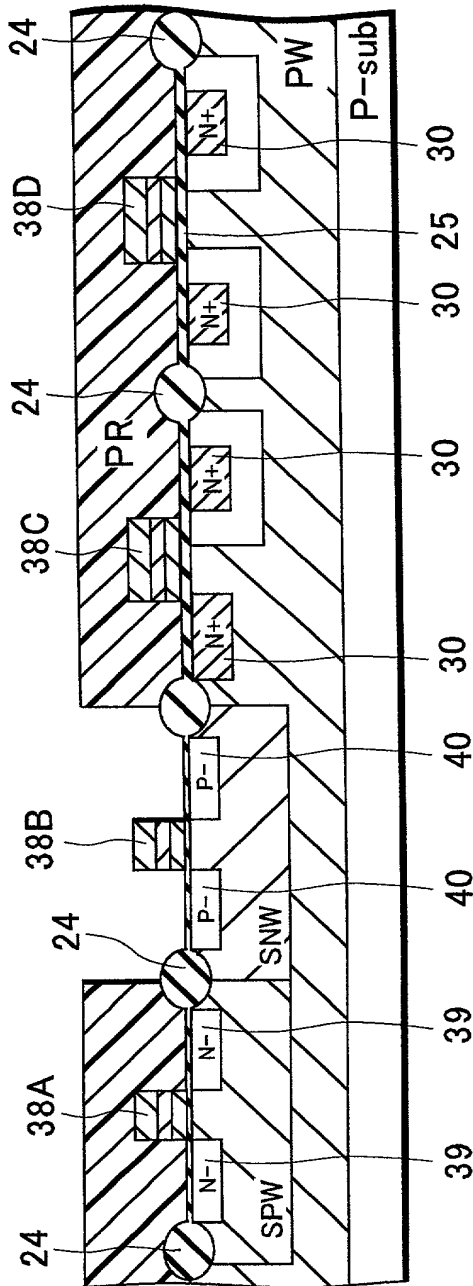
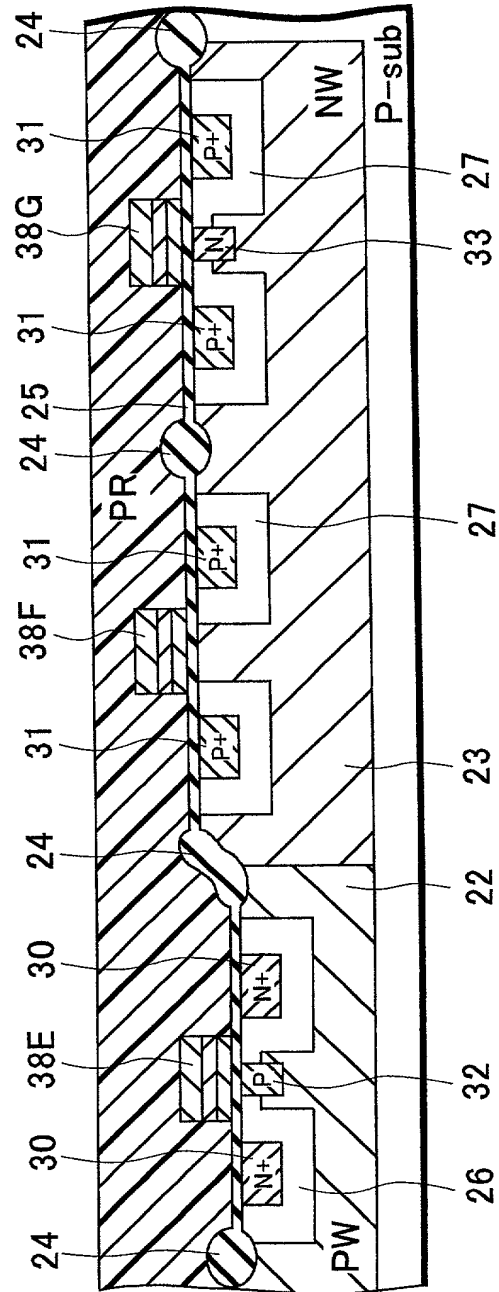


FIG.9B



This diagram shows a cross-sectional view of a semiconductor device. It features a central channel region (27) flanked by two main regions (22 and 23). The device is divided into several stages, each containing a PN junction. The stages are labeled with reference numerals: 24, 30, 38E, 30, 38F, 31, 24, 25, 31, 38G, 31, 41. The regions are labeled with material types: P-sub (P-type substrate), NW (N-type well), PR (P-type region), PW (P-type well), and N+ (N-type region). The device is shown in a cross-sectional view, with the central channel (27) and the surrounding regions (22, 23) clearly defined. The PN junctions are formed by the interface between the P-type and N-type regions.

FIG.11

(A) (B) (C)

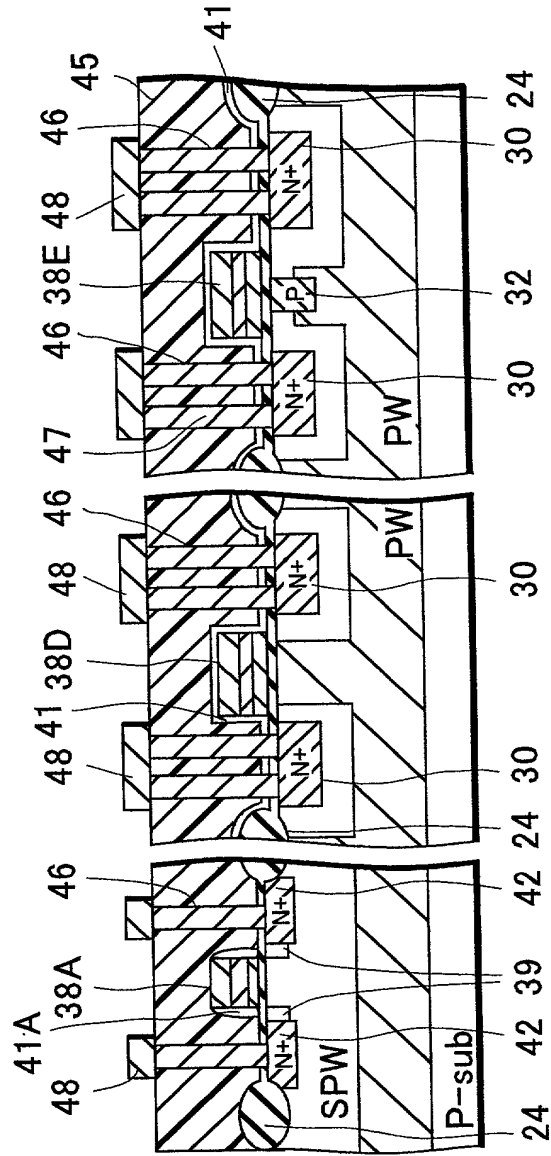
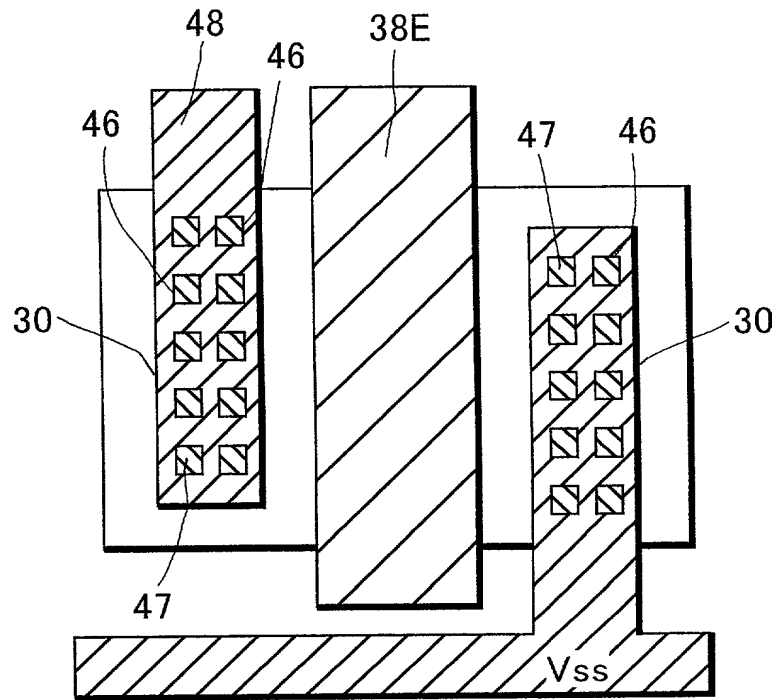


FIG. 12

[illegible]

PW

FIG. 14

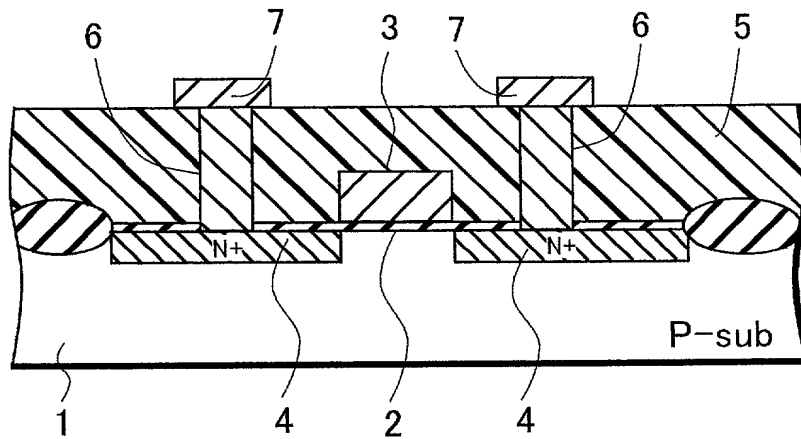


FIG. 15

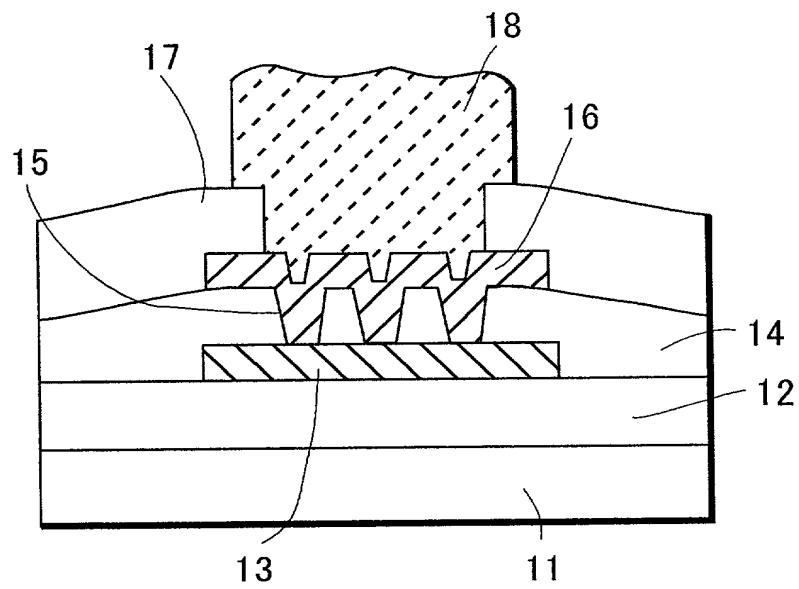


FIG. 16

